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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES M. DERDERIAN

Appeal 2009-003217
Application 09/939,258[1]
Technology Center 2800

Decided:[2] May 27, 2009

Before KENNETH W. HAIRSTON, SCOTT R. BOALICK, and THOMAS S. HAHN, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

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[1] Application filed Aug. 24, 2001. The real party in interest is Micron Technology, Inc.

[2] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1, 5-8, 10-23, 25, 28, 30-35, 53 and 54. Claims 9, 24 and 29 are withdrawn from consideration as being drawn to a non-elected invention. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellant's invention relates to semiconductor device assemblies including two or more semiconductor devices stacked relative to one another. The distance between the adjacent stacked semiconductor devices is determined by the heights of structures protruding from bond pads on an active surface of the lower semiconductor devices. (Spec. paragraph [0001].)

Claim 1 is exemplary:

1. A semiconductor device assembly, comprising:

at least one semiconductor device; and

at least one resiliently compressible spacer protruding from an active surface of the at least one semiconductor device, the at least one resiliently compressible spacer defining a distance the active surface of the at least one semiconductor device is to be spaced apart from a back side of another semiconductor device to be positioned in superimposed relation with the at least one semiconductor device.

The prior art and evidence relied upon by the Examiner in rejecting the claims on appeal is:

Eldridge	US 6,835,898 B2	Dec. 28, 2004 (filed Dec. 21, 2000)
Hikita	US 6,724,084 B1	Apr. 20, 2004 (filed Feb. 7, 2000)
Pu	US 6,593,662 B1	Jul. 15, 2003 (filed Aug. 2, 2000)
Zommer[3]	US 6,162,665	Dec. 19, 2000
Adamic	US 6,124,179	Sept. 26, 2000
Temple	US 5,654,226	Aug. 5, 1997
Inagaki	JP 59108341 A	Jun. 22, 1984

Claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53 and 54 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hikita and Eldridge.

Claims 16, 30, and 33 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hikita, Eldridge and Pu.

Rather than repeat the arguments of Appellant or the Examiner, we refer to the Answer[4] and the Briefs[5] for their respective details. Except as

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[3] Zommer, Adamic, Temple and Inagaki were cited by the Examiner for evidentiary purposes to illustrate that active devices may be formed on the "back side" of a semiconductor device. (Ans. 18.)

[4] We note that the Examiner improperly filed a second Examiner's Answer, mailed Mar. 5, 2009, which was identical to the first Examiner's Answer, mailed Aug. 28, 2008. Thus, all references in this decision will be to the first Examiner's Answer ("Ans.").

[5] We further note that the Appellant filed Reply Briefs to both Examiner's Answers. The Reply Brief filed on Oct. 28, 2008 in response to the first Examiner's Answer will be referred to as the "First Reply Br.," and the Reply Brief filed on May 5, 2009, in response to the improper second Examiner's Answer will be referred to as the "Second Reply Br."

noted in this decision, Appellant has not presented any substantive arguments directed separately to the patentability of the dependent claims. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See* 37 C.F.R. § 41.37(c)(1)(vii). Only those arguments actually made by Appellant have been considered in this decision. Arguments that Appellant did not make in the Briefs have not been considered and are deemed to be waived. *See id.*

ISSUE

First, Appellant argues that the combination of Hikita and Eldridge does not teach or suggest "an active surface of at least one semiconductor device facing the back side of another semiconductor device" (App. Br. 7), much less a "spacer defining a distance the active surface of the at least one semiconductor device is to be spaced apart from a back side of another semiconductor device" (App. Br. 7), as recited in independent claim 1.

Second, Appellant presents similar arguments that the combination of Hikita and Eldridge does not teach or suggest "a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers," as recited in claim 18. (App. Br. 7-8.)

Third, Appellant argues that "Hikita and Eldridge are limited to assemblies in which the active surfaces of two superimposed semiconductor devices face each other" (App. Br. 7; *see also* App. Br. 8) and, without the benefit of hindsight, there is no motivation "to develop an assembly in which devices with active surfaces . . . face in the same direction" (App. Br. 7; *see also* App. Br. 8).

Appellant's arguments present the following issue:

Has Appellant shown that the Examiner erred in rejecting claims 1, 5-8, 10-23, 25, 28, 30-35, 53 and 54 under 35 U.S.C. § 103(a)?

The resolution of this issue turns to the following subsidiary issues:

1. Has Appellant shown that the Examiner erred in finding that the combination of Hikita and Eldridge teaches or suggests a "spacer defining a distance the active surface of the at least one semiconductor device is to be spaced apart from a back side of another semiconductor device," as recited in independent claim 1?

2. Has Appellant shown that the Examiner erred in finding that the combination of Hikita and Eldridge teaches or suggests "a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers," as recited in independent claim 18?

3. Has Appellant shown that the Examiner erred by improperly combining the applied references?

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

Hikita

1. Hikita relates to "a semiconductor chip to be applied to a chip-on-chip structure." (Col. 1, ll. 9-10.) Hikita describes a chip-on-chip structure

with a primary chip 1 and a secondary chip 2 in a stacked relation. (Col. 11, ll. 28-31; Fig. 5.)

2. The primary chip 1 includes a front face 11 with an active surface (i.e., containing functional devices such as a transistor). (Col. 11, ll. 33-37; fig. 5.) The secondary chip 2 includes a front face 21 with an active surface. (Col. 11, ll. 47-50.) The front face 11 of the primary chip 1 is bonded to the front face 21 of the secondary chip 2. (Col. 11, ll. 45-46.)

3. The primary chip 1 and the secondary chip 2 are separated by a dummy bump BD1 and a dummy bump BD2. (Col. 12, ll. 30-33; F Fig. 5.)

Adamic

4. Adamic relates to "a fabrication method for processing circuits on two opposing planar surfaces of a semiconductor wafer." (Col. 1, ll. 13-15.) In one embodiment, Adamic describes a semiconductor circuit 100 with an elemental layer 110. (Col. 4, ll. 8-11; fig 1.) Adamic describes that "in some embodiments doped regions are generated near the backside surface 122 of element layer 110, for example, to reduce collector or drain leadout resistance, or to form junctions or ohmic contact regions." (Col. 4, ll. 24-28.)

Zommer

5. Zommer relates "to high voltage semiconductor switching devices." (Col. 1, ll. 8-9.) In one embodiment, Zommer describes forming a high voltage MOSFET on a semiconductor substrate 102 having a front surface 105 and a backside 107. (Col. 4, ll. 30-34; Fig. 3A.) Zommer further describes that "[t]o complete the device, further processing is performed by turning the wafer up-side-down and fabricating the active regions on the backside of the wafer." (Col. 4, ll. 61-63; Fig. 3B.)

Temple

6. Temple relates to a method of processing wafers for power devices. (Abstract.) Temple describes that a "wafer 10 may be partially processed on the backside to create a plurality of active areas 14 and a plurality of emitters 16." (Col. 2, ll. 64-66; Fig. 1.)

Inagaki

7. The English translation Abstract of Inagaki describes forming active regions (e.g., MOSFET devices) on a surface side and a back side of a silicon wafer.

PRINCIPLES OF LAW

On appeal, all timely filed evidence and properly presented arguments are considered by the Board. *See In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984).

In the examination of a patent application, the Examiner bears the initial burden of showing a prima facie case of unpatentability. *Id.* When that burden is met, the burden then shifts to the Applicant to rebut. *Id.*; *see also In re Harris*, 409 F.3d 1339, 1343-44 (Fed. Cir. 2005) (finding rebuttal evidence unpersuasive). If the Applicant produces rebuttal evidence of adequate weight, the prima facie case of unpatentability is dissipated. *Piasecki*, 745 F.2d at 1472. Thereafter, patentability is determined in view of the entire record. *Id.* However, on appeal to the Board it is the Appellant's burden to establish that the Examiner did not sustain the necessary burden and to show that the Examiner erred. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [for obviousness] by showing insufficient evidence of *prima facie* obviousness or by rebutting the *prima facie* case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

During examination of a patent application, a claim is given its broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.,* 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313.

ANALYSIS

We do not find Appellant's arguments that the Examiner erred in rejecting claims 1, 5-8, 10-23, 25, 28, 31, 32, 34, 35, 53 and 54 under 35 U.S.C. § 103(a) as being obvious over Hikita and Eldridge to be meritorious. Nor do we find merit in Appellant's arguments that the Examiner erred in combining Hikita and Eldridge. In addition, we do not find Appellant's arguments that the Examiner erred in rejecting claims 16, 30 and 33 under 35 U.S.C. § 103(a) as being obvious over Hikita, Eldridge and Pu to be meritorious.

Claims 1, 5-8, 10-17 and 53

Appellant's arguments (App. Br. 6-7; First Reply Br. 2-3; Second Reply Br. 3-4) that the combination of Hikita and Eldridge does not teach or suggest a "spacer defining a distance the active surface of the at least one semiconductor device is to be spaced apart from a back side of another semiconductor device," as recited in independent claim 1, are not persuasive.

The Examiner found that the primary chip 1 of Hikita corresponds to the claimed "semiconductor device," dummy bumps BD1 and BD 2 correspond to the claimed "spacer," and the secondary chip 2 corresponds to the claimed "another semiconductor device." (Ans. 4; FF 1-3.) The Examiner also found that Hikita teaches "a back side of another semiconductor device" because the secondary chip 2 contains a "back side" (i.e., reverse side) relative to an opposite side. (Ans. 12-13.) We agree with the Examiner.

Under the broadest reasonable interpretation consistent with the Specification, we agree with the Examiner that Hikita teaches the limitation

of "a back side of another semiconductor device." Appellant argued that a "back side" is a side of a semiconductor device opposite to an "active side" that does not contain integrated circuitry. (App. Br. 7; First Reply Br. 2-3; Second Reply Br. 3-4.) However, the scope of the claim is not so narrow. The relevant plain meaning of "back" is "the side or surface opposite the front or face" or "reverse side." *Merriam-Webster's Collegiate Dictionary* 83 (10th ed. 1996). We agree with the Examiner that Hikita teaches a "back side" of the secondary chip 2 as the front face 21 because the front face 21 is a "back side" relative to a surface opposite the front face 21 (*see* FF 2). Moreover, "back side" is a relative term and the Specification does not provide any reference side for determining the "back side" of a semiconductor device. Thus, we find the Examiner's construction of "back side" to be reasonable and consistent with the Specification. Appellant has not pointed to any special definition of "back side" in the Specification that would require a different interpretation.

We note that to support the position that "a back side and an active surface [of a semiconductor device] are not mutually exclusive" (Ans. 18), the Examiner cited Zommer, Adamic, Temple and Inagaki, which teach forming an active device on the "back side" of a semiconductor device (Ans. 18; *see* FF 4-7). Appellant argues that Zommer, Adamic, Temple and Inagaki further illustrate that a "back side" is the side opposite an active side. (Second Reply Br. 2-3.) However, this argument is not convincing because as discussed above, "back side" is a relative term and the Specification does not provide any reference side for determining the "back side" of a semiconductor device. Moreover, claim 1 does not require the active surfaces to face in the same direction. We further note that Appellant

submitted rebuttal evidence[6] to support the position that a "back side" of a semiconductor device does not contain integrated circuitry. (First Reply Br. 2-3; Second Reply Br. 3-4.) However, Appellant's evidence only illustrates several instances in which a "back side" does not contain integrated circuitry. (First Reply Br. 2-3; Second Reply Br. 3-4) Such evidence does not rebut the Examiner's position that integrated circuitry can be formed on the "back side" of a semiconductor device. (*See* FF 4-7).

We further note that Appellant argued that there is no motivation "to develop an assembly in which devices with active surfaces . . . face in the same direction." (App. Br. 7.) However, because the rejection of claim 1 is not based on modifying Hikita to invert the secondary chip 2 relative to the primary chip 1 (i.e., modifying Hikita such that the front faces 21 and 22 face in the same direction rather than in opposite directions), Appellant's arguments regarding the lack of motivation are not germane. Claim 1 does not require the active surfaces to face in the same direction. As discussed, an active surface may be formed on the "front side" or the "back side" of a semiconductor device.

Therefore, Appellant has not shown that the Examiner erred in finding that the combination of Hikita and Eldridge teaches or suggests a "spacer defining a distance the active surface of the at least one semiconductor

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[6] Appellant cites column 1, lines 62-64 of U.S. Patent No. 6,828,175 ("The component includes a semiconductor die having a thinned semiconductor substrate with a circuit side (front side) and a back side") and column 4, lines 17-23 of U.S. Patent No. 6,096,568 ("The die paddle 108 is removed in order to fully expose the back side 126 of the die 110. . . Other processes can then be used to mill the back side of the die 110. . . .") as rebuttal evidence. (Reply Br. 2-3.)

device is to be spaced apart from a back side of another semiconductor device," as recited in independent claim 1.

We conclude that Appellant has not show that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 103(a). Because Appellant has not presented arguments regarding claims 5-8, 10-17 and 53, we affirm the rejection of these claims under 35 U.S.C. § 103(a) for the same reasons as claim 1, from which they depend.

Claims 18-23, 25, 28, 31, 32, 34, 35 and 54

Appellant's arguments (App. Br. 7-8; First Reply Br. 3; Second Reply Br. 4-5) that the combination of Hikita and Eldridge does not teach or suggest "a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers," as recited in independent claim 18, are not persuasive.

The Examiner found that the primary chip 1 of Hikita corresponds to the claimed "first semiconductor device," dummy bumps BD1 and BD2 correspond to the claimed "discrete spacers," and the secondary chip 2 corresponds to the claimed "second semiconductor device." (Ans. 6; FF 1-3.) The Examiner found that Hikita teaches the "second semiconductor device comprising a back side positioned on . . . the discrete spacers" because the secondary chip 2 contains a "back side" (i.e., reverse side) relative to an opposite side. (Ans. 12-13.)

Similar to the previous discussion of claim 1, under the broadest reasonable interpretation consistent with the Specification, we agree with the Examiner that Hikita teaches the limitation of a "second semiconductor device comprising a back side positioned on the . . . discrete spacers."

Likewise, similar to the previous discussion of claim 1, Appellant's arguments (App. Br. 8) that there is no motivation to combine Hikita and Eldridge are not germane.

Therefore, Appellant has not shown that the Examiner erred in finding that the combination of Hikita and Eldridge teaches or suggests "a second semiconductor device comprising a back side positioned on the mutually laterally spaced discrete spacers," as recited in independent claim 18.

We conclude that Appellant has not shown that the Examiner erred in rejecting claim 18 under 35 U.S.C. § 103(a). Because Appellant has not presented arguments regarding claims 19-23, 25, 28, 31, 32, 34, 35 and 54, we affirm the rejection of these claims under 35 U.S.C. § 103(a) for the same reasons as claim 18, from which they depend.

Claims 16, 30 and 33

Although Appellant nominally argues the rejection of dependent claims 16, 30 and 33 separately (App. Br. 8), the arguments presented do not point out with particularity or explain why the limitations of the dependent claims are separately patentable. Instead, Appellant summarily alleges that these claims "[are] allowable . . . for depending either directly or indirectly from independent claim 18." (App. Br. 8.) Because Appellant has not persuasively rebutted the Examiner's prima facie case of obviousness for dependent claims 16, 30 and 33 based on the teachings of Hikita, Eldridge and Pu, we will sustain the rejection of claims 16, 30 and 33 for the reasons discussed with respect to independent claims 1 and 18, from which claims 16, 30 and 33 depend.

CONCLUSION

Based on the findings of facts and analysis above, we conclude that:

Appellant has not shown that the Examiner erred in rejecting claims 1, 5-8, 10-23, 25, 28, 30-35, 53 and 54 under 35 U.S.C. § 103.

DECISION

The rejection of claims 1, 5-8, 10-23, 25, 28, 30-35, 53 and 54 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

rvb

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